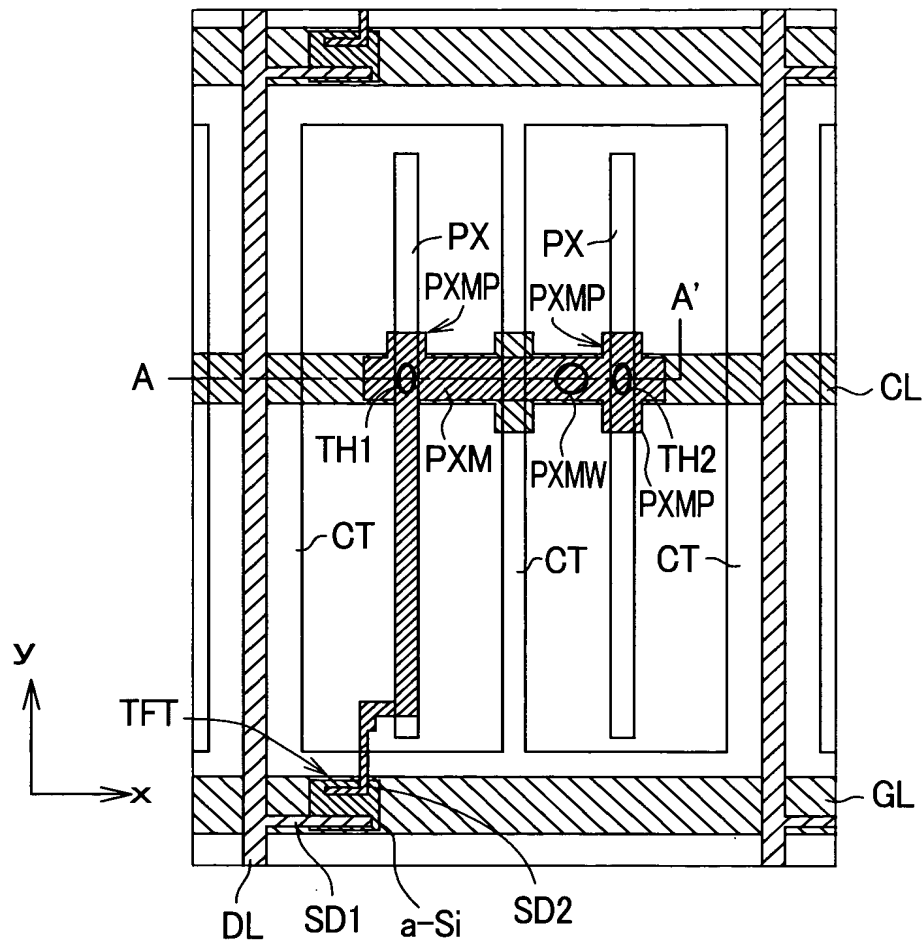
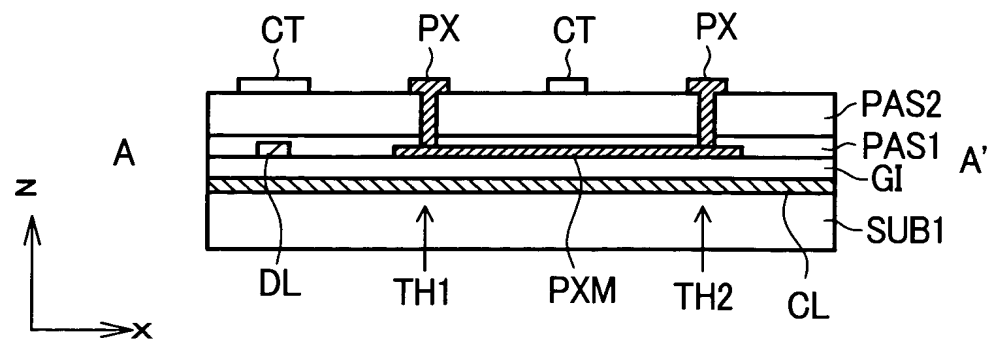


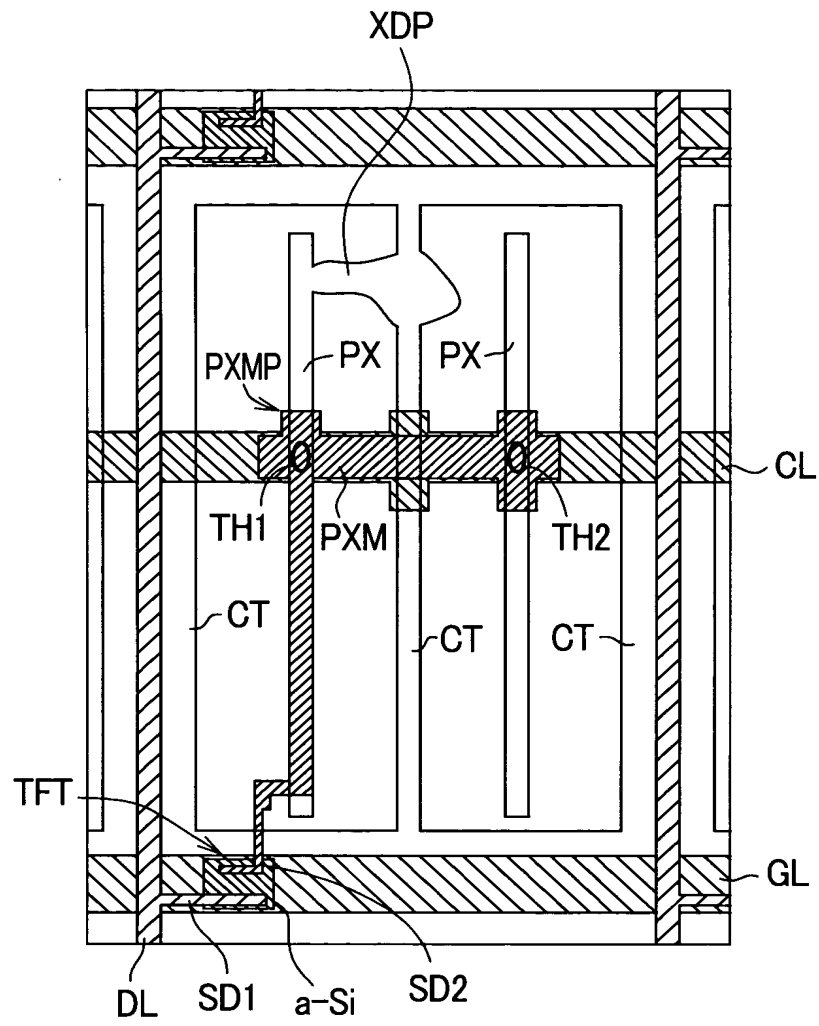
*FIG. 1A*



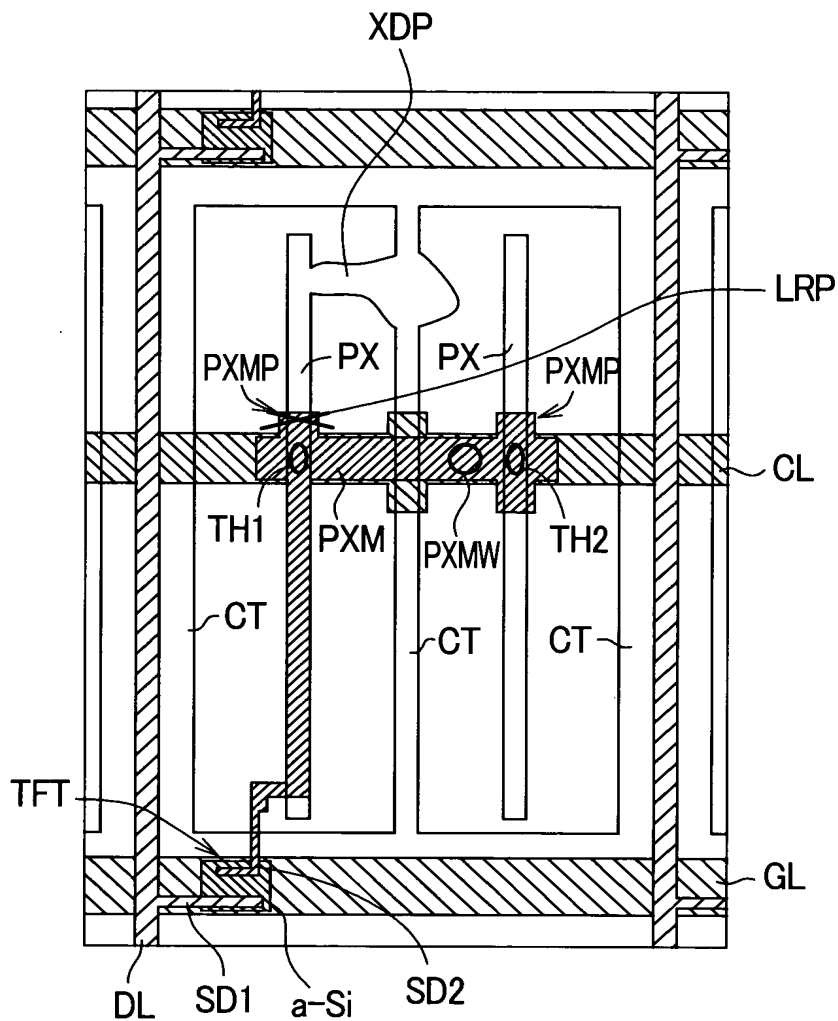
*FIG. 1B*



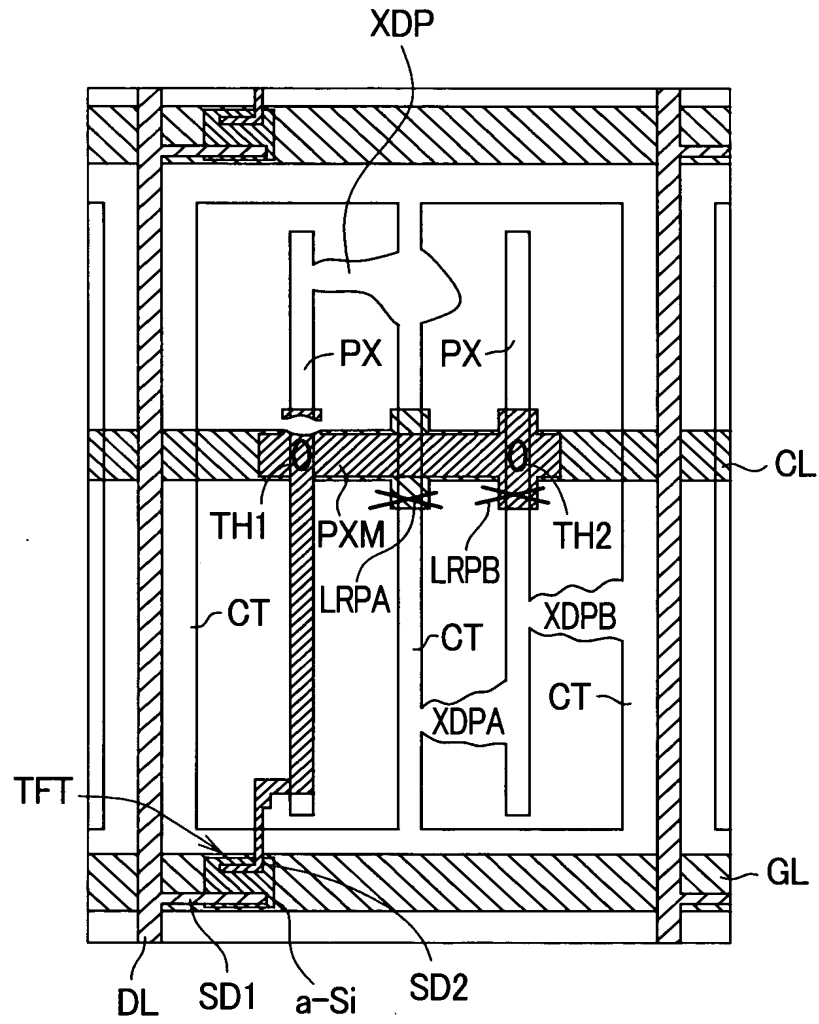
*FIG. 2*



*FIG. 3*

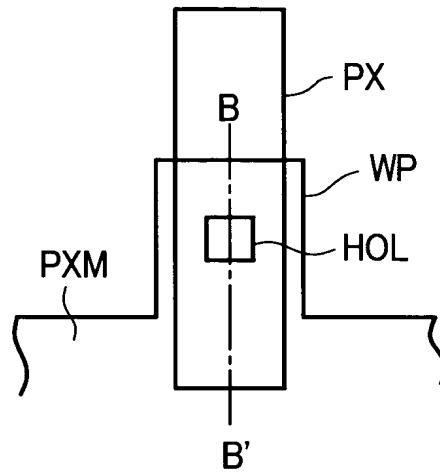


**FIG. 4**

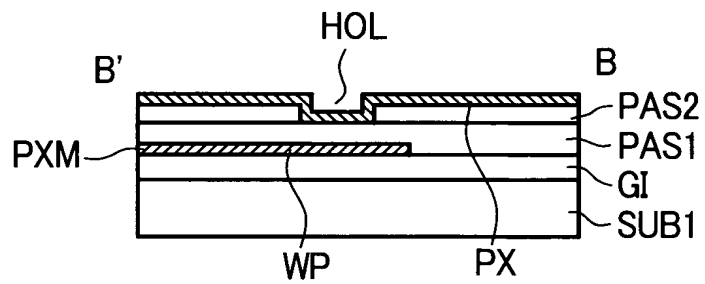




*FIG. 7A*



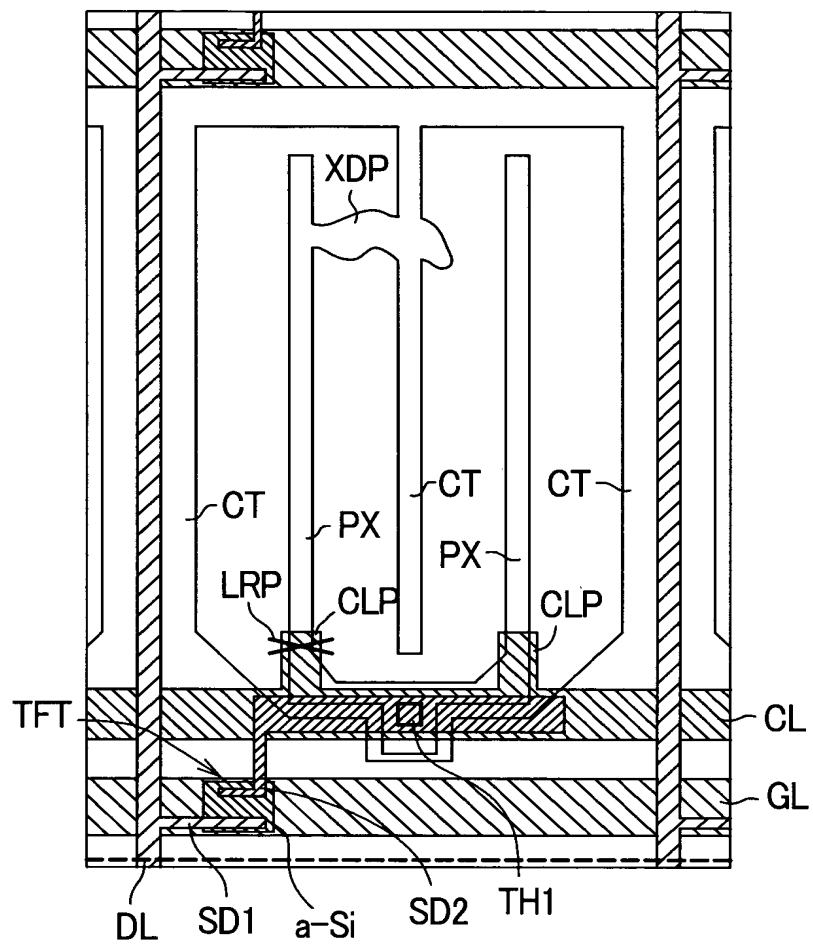
*FIG. 7B*



A detailed cross-sectional diagram of a TFT-LED device. The structure is built on a substrate with a bottom layer labeled 'DL' (dielectric layer). Above this is a layer of 'a-Si' (amorphous silicon). The device features two TFTs (Thin-Film Transistors) and an LED structure. The TFTs are labeled 'TFT' and 'SD1' and 'SD2' (source-drain regions). The LED structure includes a p-type layer 'PXM' (p-type material) and an n-type layer 'IM' (intrinsic material). The TFTs are connected to the LED structure via 'CT' (contact) and 'PX' (p-type) regions. The device is surrounded by a frame labeled 'CL' (cladding layer) and 'GL' (glass layer). Other labels include 'TH1', 'TH2', 'C', 'C'', 'XDP', and 'IM'.

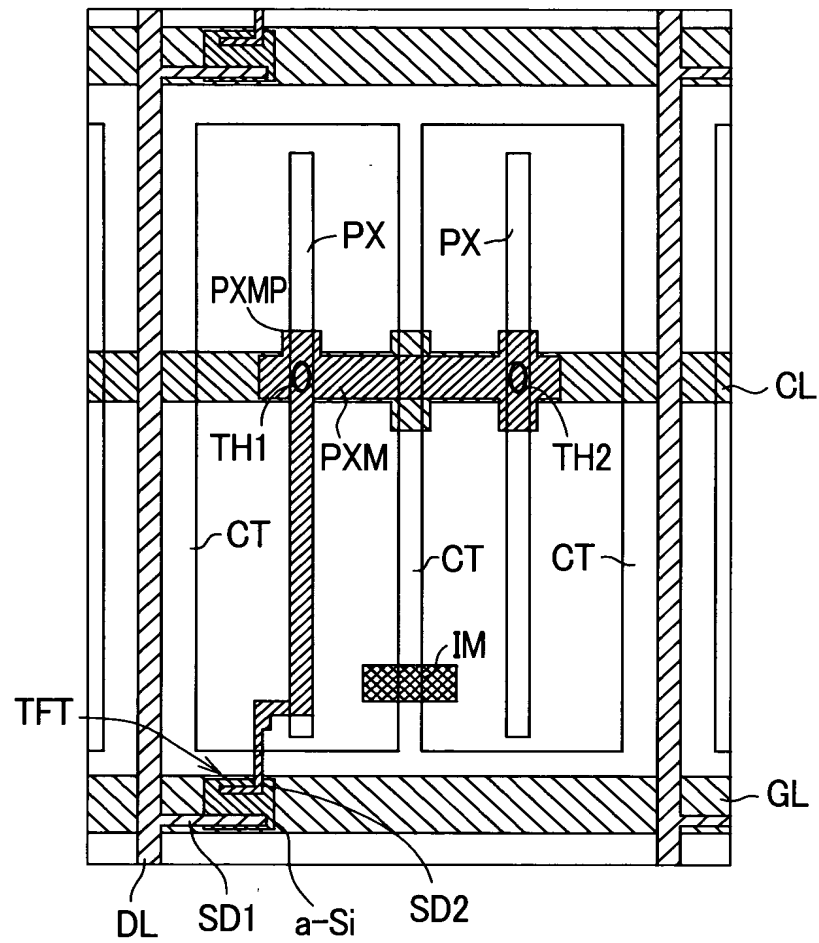
Fig. 1 is a cross-sectional view of a semiconductor device. The device includes a substrate (SUB1) with a gate insulator (GI) layer. A gate electrode (IM) is formed on the GI layer. A passivation layer (PAS1) is formed on the gate electrode. A second passivation layer (PAS2) is formed on the PAS1 layer. A pixel electrode (PX) is formed on the PAS2 layer.

*FIG. 9*

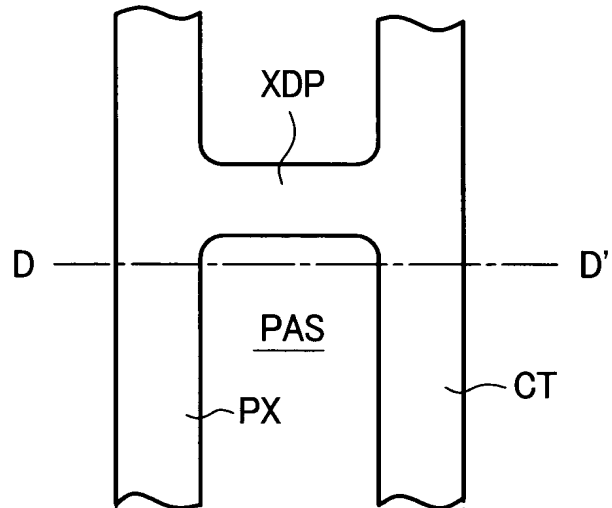




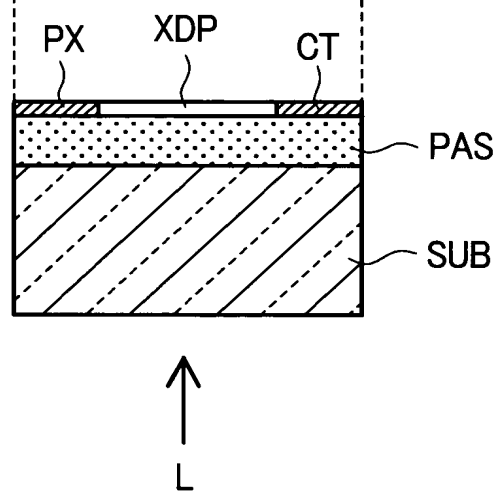
*FIG. 10*



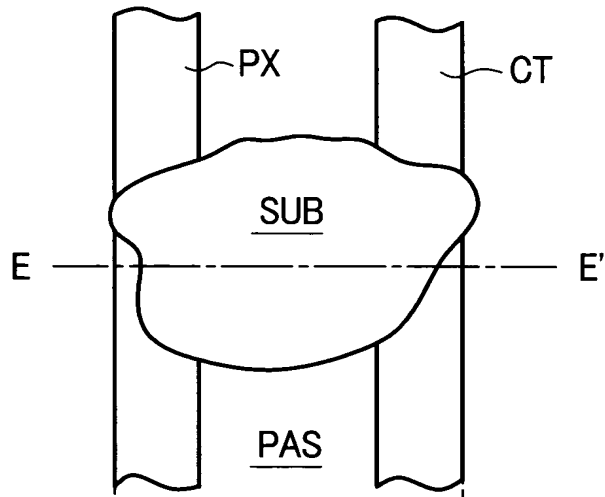
*FIG. 11A*



*FIG. 11B*



**FIG. 12A**



**FIG. 12B**

